Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-18 (canceled)

Claim 19 (currently amended): A method for forming an electrical interconnection structure for connection to large electrical contacts, the method comprising:

providing a semiconductor substrate having a copper-containing pad layer formed thereon such that the copper-containing pad layer includes a plurality of elongate slots having a long axis, a short axis, and sidewalls, the slots extending through the pad layer to expose the underlying semiconductor substrate;

forming, over the pad layer, a dielectric layer having a plurality of elongate openings formed therein, the elongate openings having a long axis, a short axis, and sidewalls and are configured to extend into the dielectric layer to a depth **sufficient to expose the sidewalls of the slots in the copper-containing pad layer all the way down to the underlying semiconductor substrate** ~~**such that substantial portions of the sidewalls of the elongate slots of the copper-containing pad layer are exposed**~~, thereby enabling electrical connections to the underlying copper-containing pad layer;

forming elongate copper-containing contacts in the plurality of elongate openings, said contacts physically contacting the exposed portions of the sidewalls thereby establishing electrical connections to the underlying copper-containing pad layer; and

conducting further processing as needed.

Claim 20 (withdrawn): A method as in Claim 19 wherein the step of forming the dielectric layer comprises forming the dielectric layer such that the long axis of the elongate slots lies substantially parallel to the long axis of the elongate trenches in the pad layer to expose a portion of the sidewalls of the elongate trenches of the pad layer.

Claim 21 (withdrawn): A method as in Claim 20 wherein the step of forming elongate copper-containing contacts in the plurality of elongate trenches includes the steps of:

forming at least one barrier layer in the elongate slots;

forming a seed layer in the elongate slots;

forming a bulk copper-containing layer on the seed layer; and

wherein the step of conducting further processing includes removing excess copper-containing materials from a surface of the dielectric layer and electrically connecting the elongate copper-containing contacts to other circuit elements.

Claim 22 (withdrawn): A method as in Claim 21 wherein the step of conducting further processing includes forming other semiconductor circuit structures.

Claim 23 (previously presented): A method as in Claim 19 wherein the step of forming the dielectric layer comprises forming the dielectric layer such that the long axis of the elongate openings of the dielectric layer lie transverse to the long axis of the elongate slots of the pad layer thereby exposing the substantial portions of the sidewalls of the pad layer.

Claim 24 (original): A method as in Claim 23 wherein the step of forming elongate copper-containing contacts in the plurality of elongate trenches includes the steps of:

forming at least one barrier layer in the elongate slots;

forming a seed layer in the elongate slots;

forming a bulk copper-containing layer on the seed layer; and

wherein the step of conducting further processing includes removing excess copper-containing materials from a surface of the dielectric layer and electrically connecting the elongate copper-containing contacts to other circuit elements.

Claim 25 (original): A method as in Claim 24 wherein the step of conducting further processing includes forming other semiconductor circuit structures.

Claim 26 (currently amended): A method for forming an electrical interconnection structure for connection to large electrical contacts, the method comprising:

providing a semiconductor substrate having a conductive pad layer formed thereon such that the copper-containing pad layer includes a plurality of elongate slots having a long axis, a

short axis, and sidewalls, the slots extending through the pad layer to expose the underlying semiconductor substrate;

forming a dielectric layer over the pad layer;

forming a plurality of elongate trenches in the dielectric layer, the elongate trenches having a long axis, a short axis, and sidewalls and are configured to such that the long axis of the elongate trenches lies transverse to the long axis of the elongate slots in the pad layer to expose **portions of the sidewalls of the elongate slots of the pad layer to a depth that extends all the way down to the underlying semiconductor substrate** ~~a substantial portion of the sidewalls of the elongate slots of the pad layer~~ and wherein the trenches extend sufficiently deep into the dielectric layer so that electrical connections to the underlying conductive pad layer can be formed; and

filling the elongate trenches of the dielectric layer with a conductive material to form conductive contacts which for electrical contacts with the **exposed** ~~substantial~~ portions of the sidewalls and tops of the conductive pad, thereby establishing electrical connections to the underlying conductive pad layer.

Claim 27 (previously presented): A method as in Claim 26 wherein the step of filling the plurality of elongate trenches includes the steps of:

forming at least one barrier layer in the elongate slots;

forming a seed layer in the elongate slots;

forming a bulk copper-containing layer on the seed layer; and

removing excess copper-containing materials from a surface of the dielectric layer and electrically connecting the elongate copper-containing contacts to other circuit elements.

Claim 28 (previously presented): A method as in Claim 27 further including the operation of conducting further processing as needed.

Claim 29 (previously presented): A method as in Claim 28 wherein the operation of conducting further processing includes forming electrical connections to other semiconductor circuit structures.

Claim 30 (previously presented): A method as in Claim 28 wherein the operation of conducting further processing includes forming an electrically conductive top pad on the dielectric layer wherein the top pad is electrically connected with the conductive contacts.

Claim 31 (cancelled).

Claim 32 (cancelled).

Claim 33 (new): A method for forming an electrical interconnection structure for connection to large electrical contacts, the method comprising:

providing a semiconductor substrate having a copper-containing pad layer formed thereon such that the copper-containing pad layer includes a plurality of elongate slots having a long axis, a short axis, and sidewalls, the slots extending through the pad layer to expose the underlying semiconductor substrate;

forming, over the pad layer, a dielectric layer having a plurality of elongate openings formed therein, the elongate openings having a long axis, a short axis, and sidewalls and are configured to extend into the dielectric layer to a depth sufficient to expose a portion of at least one of the sidewalls of the slots of the copper-containing pad layer, wherein the exposed portion extends a majority of the distance down the sidewall toward the underlying semiconductor substrate, thereby enabling electrical connections to the underlying copper-containing pad layer;

forming elongate copper-containing contacts in the plurality of elongate openings, said contacts physically contacting the exposed portions of the sidewalls thereby establishing electrical connections to the underlying copper-containing pad layer; and

conducting further processing as needed.

Claim 34 (new): A method for forming an electrical interconnection structure for connection to large electrical contacts, the method comprising:

providing a semiconductor substrate having a conductive pad layer formed thereon such that the copper-containing pad layer includes a plurality of elongate slots having a long axis, a short axis, and sidewalls, the slots extending through the pad layer to expose the underlying semiconductor substrate;

forming a dielectric layer over the pad layer;

forming a plurality of elongate trenches in the dielectric layer, the elongate trenches having a long axis, a short axis, and sidewalls and are configured to such that the long axis of the elongate trenches lies transverse to the long axis of the elongate slots in the pad layer to expose a portion of at least one of the sidewalls of the slots in the copper-containing pad layer, wherein the exposed portion extends a majority of the distance down the sidewall toward the underlying semiconductor substrate and wherein the trenches extend sufficiently deep into the dielectric layer so that electrical connections to the underlying conductive pad layer can be formed; and

filling the elongate trenches of the dielectric layer with a conductive material to form conductive contacts which for electrical contacts with the **exposed** portions of the sidewalls and tops of the conductive pad, thereby establishing electrical connections to the underlying conductive pad layer.